Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of claims:

1. (Previously Presented) A processor, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

an instruction processing system coupled to the instruction cache, having a power control input coupled to the hit/miss output of the UOP cache.

2. (Previously Presented) The processor of claim 1, wherein the instruction cache comprises a cache lookup unit and a cache fetch unit, the cache fetch unit having a power control input coupled to the hit/miss output of the UOP cache.

3. (Currently Amended) The processor of claim 1, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to the power control input.

4. (Previously Presented) The processor of claim 1, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss output.

5. (Previously Presented) The processor of claim 4, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit.

6. (Previously Presented) The processor of claim 5, wherein the delay element is associated with a delay corresponding to a processing time of the instruction processing system.

7.-9. (Cancelled)

10. (Previously Presented) A apparatus, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, wherein the UOP cache includes an output for a hit/miss indicator,

wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to unpower the data fetch unit selectively.

11. (Previously Presented) The apparatus of claim 10, further comprising an instruction processing system in communication with the instruction cache, the hit/miss indicator to unpower the instruction processing system selectively.

12. (Previously Presented) The apparatus of claim 11, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to the hit/miss indicator.

13. (Previously Presented) The apparatus of claim 10, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss indicator.

14. (Previously Presented) The apparatus of claim 13, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

15. (Previously Presented) The front-end processing system of claim 14, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processing system.

16.-26. (Canceled)

27. (Currently Amended) A method, comprising:

providing an address in parallel to a micro-instruction cache and to an instruction processing system;

if the address hits the instruction processing system, then, within the instruction processing system:

outputting addressed data from an instruction cache performing instruction synchronization of the output data, and

decoding instructions obtained therefrom to obtain decoded micro-instructions; and

if the address hits the micro-instruction cache, then:

outputting addressed micro-instructions from the micro-instruction cache, and

terminating ~~the foregoing~~ performance of the outputting and the decoding operations of the instruction processing system, if any, that result from the providing of the address to the instruction processing system.

28. (Previously Presented) The method of claim 27, wherein the terminating further comprises withholding clock signals from the instruction processing system.

29. (Previously Presented) The method of claim 27, wherein the terminating further comprises generating a disabling output signal from the micro-instruction cache to the instruction cache.

30. (Previously Presented) The method of claim 27, further comprising delaying outputting the addressed micro-instructions from the micro-instruction cache by an amount representing a difference between processing time of the instruction processing system and processing time of the micro-instruction cache.

31. (Currently Amended) A method, comprising:

applying an address in parallel to first and second caches, the caches storing data in mutually different formats,

if the address hits the second cache, then:

outputting addressed data from the second cache, and

converting the output data to a format of the first cache;

if the address hits the first cache, then:

outputting addressed data therefrom, and

terminating performance of the outputting [[,]] and the converting operations of the second cache, if any, that result from the applying of the address to the second cache.

32. (Currently Amended) The method of claim 31, wherein the terminating further comprises withholding clock signals from the ~~instruction processing system~~ second cache.

33. (Currently Amended) The method of claim 31, wherein the terminating further comprises generating a disabling output signal from the ~~micro-instruction~~ first cache to the ~~instruction~~ second cache.

34. (Currently Amended) The method of claim 31, further comprising delaying outputting the addressed ~~micro-instructions~~ data from the ~~micro-instruction~~ first cache by an amount representing a difference between processing time of the ~~instruction processing system~~ second cache and processing time of the ~~micro-instruction~~ first cache.

35. (Currently Amended) A system, comprising:

a processor for performing instruction pre-processing and to output decoded instructions, the processor comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

the instruction cache having a first cache lookup unit and a data fetch unit, and

the hit/miss indicator to selectively disable the data fetch unit, and

an execution unit to receive and execute the decoded instructions from the processor.

36. (Previously Presented) The system of claim 35, further comprising a memory to store and retrieve data associated with the decoded instructions.

37. (Previously Presented) The system of claim 35, further comprising an instruction processor in communication with the instruction cache, the hit/miss indicator to unpower the instruction processor selectively.

38. (Previously Presented) The system of claim 37, wherein the instruction processor comprises an instruction synchronizer and an instruction decoder coupled to the hit/miss indicator.

39. (Currently Amended) The system of claim 35, wherein the UOP cache comprises a second cache lookup unit and a cache fetch unit, the second cache lookup unit coupled to the hit/miss indicator.

40. (Currently Amended) The system of claim 39, wherein the UOP cache further comprises a delay element provided between the second cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

41. (Previously Presented) The system of claim 40, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processor.